Amendments to the Specification:

Please replace paragraphs [0015], [0016], [0017], [0038], [0049], [0060], [0070], [0073] with the following amended paragraphs:

[0015] A PLA in accordance with an embodiment of the invention is designed after knowing the initial logic to be implemented by the PLA. Once such logic is known, a PLA sized specifically to that logic is modelled. Then unnecessary programmable connections are removed creating a relatively small, but fast PLA to implement the given function. Additional programmable connections are then re-added to the model to allow for future reprogramming. Finally, the modelled PLA is constructed.

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[0016] The result is a PLA that achieves a maximum amount of depopulation while still implementing a logic function and maintaining flexibility for future reprogramming. In addition a PLA in accordance with an embodiment of the invention can be built so that no matter what functionality is programmed, the performance characteristics for the device remain the same.

[0017] A PLA in accordance with an embodiment of the invention does not require a regular array structure. Therefore, such a PLA is flexible for place and route considerations, particularly when integrated with other logic in larger circuits.

[0038] Thus, in accordance with an embodiment of the invention, selected programmable connections (e.g, intersections) of a PLA are removed, "depopulating" the PLA, to minimize the space and maximize the speed of the PLA. The connections that are removed are connections that will not be used in by the functionality to be initially programmed in the PLA. Nonetheless, certain initially unnecessary programmable connections are selectively placed in the array to allow for future reprogramming of the array with functionality different then that initially intended.

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[0049] In sum, in accordance with an embodiment of the invention, a description of functionality to be implemented in a PLA is received by a program such as a PLA compiler. The description is analyzed and a fully populated PLA is modeled. Then, either the OR array, the AND array, or both are depopulated to remove all unnecessary programmable connections in the model. Strategically selected intersections are then repopulated within the model with programmable connections to allow for future reprogramming. Finally, the PLA is physically constructed based on the modelled PLA.

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[0060] Both the embodiments illustrated in Figs. 13 and 14 are advantageous over wired-OR structures such as those of Fig. 2. First, the structures of Figs. 13 and 14 do not require a regular array structure. Therefore, a PLA in accordance with an embodiment of the invention can be made as small as possible without the limitations of a regular array structure. In some situations, portions of the PLA can even be intermixed with other circuitry in a larger custom chip, such as an ASIC described in Application Serial No.09/512,783, filed February 25, 2000, and entitled "Programmable Logic Array Embedded in Mask-Programmed ASIC." Still, even if all portions of the PLA are located in proximity to one another, these portions can be scrambled. Thus, although a PLA in accordance with an embodiment of the invention appears to have a regular structure in the figures, such regularity is shown only for clarity of description. In its physical implementation, a PLA in accordance with an embodiment of the invention need not have any regular structure nor resemble its conventional counterparts at all.

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[0070] AND trees and OR trees (as well as buffer trees) have been mentioned above. When building a PLA in accordance with an embodiment of the invention these trees can be built on the fly as needed by the PLA compiler (the program that analyzes the input PLA description and then generates a structural netlist for the PLA). Alternatively, AND and OR trees can be limited to a predefined set of gate primitives used for building trees. Such primitives may be designed such that certain pins/inputs for the primitives are favored due to their speed advantage (e.g., those pins/inputs towards the end of the tree), which will be useful in determining where to add in shared/spare p-terms. Still another method for

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generating trees is to create a library of all possible trees that will be needed using a synthesis tool like Synopsys Design Compiler as is known in the art. The trees would be synthesized for maximum speed and the tree of the required size would be chosen at the time the PLA is constructed. Again, such trees could be designed such that certain pins/inputs are favored due to their speed advantage.

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[0073] Therefore, a device has been described that allows the formation of smaller, faster, yet flexible PLAs. Unlike conventional "folding" techniques, a device in accordance with an embodiment of the invention requires no regular array structure. Further, distinct from folding, a device in accordance with an embodiment of the invention can depopulate the PLA to a maximum, but then selectively repopulate to allow for future flexibility in reprogramming.